Journal of Network and Computer Applications 34 (2011) 517–522

Contents lists available at ScienceDirect

Journal of Network and Computer Applications

journal homepage: www.elsevier.com/locate/jnca

Review

A survey of memory error correcting techniques for improved reliability

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ARTICLE INFO

Article history:
Received 29 April 2010
Received in revised form
6 September 2010
Accepted 18 November 2010
Available online 24 November 2010

Keywords:
Computer in critical applications
Memory errors
Logic errors
Error correction techniques
System reliability
Miniaturization

ABSTRACT

Computer systems failure due to hard or soft memory errors is very common. Hard errors are caused due to any permanent fault in the memory chips whereas soft errors in memory chips, generally transients or intermittent in nature, are caused due to alpha particles or cosmic rays. Non-critical systems may not require serious attention for such failures where simple, cost-effective, little-overhead techniques may be considered enough. However, semi/fully critical systems do require a careful treatment, keeping aside all other factors, but the reliability and serviceability during the intended period of time. A number of monolithic and hybrid techniques have been developed over the years. This paper aims to expose the concerns related to increasing memory and logic errors as an off-shoot due to the advancement in technologies. A survey is presented regarding the techniques being used to deal with such errors.

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1. Introduction

Due to the miniaturizations in process technology, which is expected to scale below 40 nm and 12 Gb/cm^2 by the year 2012, the designers of memory chips have been facing the new reliability threats in terms of increased probability of “Logic Errors” and “Memory Errors”, of which latter is pre-dominant over the former. The failure rate is defined as 1 FIT (failure in time), if a device fails in 10^9 h. In case of electronic memory it is measured as FIT/MB, which is equivalent to 1 upset per 10^9 h per 10^6 bits.

Considering a conservative error rate of 500 FIT Mbit, a memory of 1 GB in a system may get an error every two weeks, extrapolating this to a memory of Terabyte in future may experience an error every few minutes.

Beside miniaturizations, high switching speed is another threat to the reliability. According to a survey, the factors that cause to increase error rates (both logic errors and memory errors) are:

- increased complexity (Johnston (JPL), 2000a, 2000b; Shivakumar et al., 2002; Normand, 1966);
- higher density of chips (Johnston (JPL), 2000a, 2000b; Ziegler, 2000, 1996; Cataldo, 1998);
- lower operating voltages (Johnston (JPL), 2000b; Ziegler, 2000, 1996; Cataldo 1998; Holbert, 2003);
- higher speeds (lower latencies) (Johnston (JPL), 2000a, 2000b; Shivakumar et al., 2002; Cataldo, 1998; Holbert, 2003);
- lower cell capacitance (Johnston (JPL), 2000a, 2000b; Cataldo, 1998; Graham, 2002).

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1084-8045/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.jnca.2010.11.006