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Thermal Cycling Reliability of Sn-Ag-Cu Solder Interconnections—Part 2: Failure Mechanisms

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Part 1 of this study focused on identifying the effects of (i) temperature difference (ΔT), (ii) lower dwell temperature and shorter dwell time, (iii) mean temperature, (iv) dwell time, and (v) ramp rate on the lifetime of ball grid array (with 144 solder balls) component boards. Based on the characteristic lifetime, the studied thermal cycling profiles were categorized into three groups: (i) highly accelerated conditions, (ii) moderately accelerated conditions, and (iii) mildly/nonaccelerated conditions. In this work, the observed differences in component board lifetime are explained by studying the failure mechanisms and microstructural changes that take place in the three groups of loading conditions. It was observed that, under the standardized thermal cycling conditions (highly accelerated conditions), the networks of grain boundaries formed by recrystallization provided favorable paths for cracks to propagate intergranularly. It is noteworthy that the coarsening of intermetallic particles was strong in the recrystallized regions (the cellular structure had disappeared completely in the crack region). However, under real-use conditions (mildly/nonaccelerated conditions), recrystallization was not observed in the solder interconnections and cracks had propagated transgranularly in the bulk solder or between the intermetallic compound (IMC) layer and the bulk solder. The real-use conditions showed slight coarsening of the microstructure close to the crack region, but the solder bulk still included finer IMC particles and β-Sn cells characteristic of the as-solidified microstructures. These findings suggest that standardized thermal cycling tests used to assess the solder interconnection reliability of BGA144 component boards create failure mechanisms that differ from those seen in conditions representing real-use operation.

Key words: Reliability, thermal cycling, thermal shock, microstructure, recrystallization, accelerated lifetime test

INTRODUCTION

Electronic devices experience significant changes in temperature during normal operation due to internal heat dissipation and variation of the ambient temperature. As component boards inside are exposed to temperature changes, strains and stresses concentrate in the solder interconnections as the natural expansion/contraction of the printed wiring board (PWB) is restricted by the packages. Thermomechanical reliability is typically characterized by performing thermal cycling tests in which various parameters such as dwell time, ramp rate, and temperature extremes are used to accelerate real operation conditions. There are, however, risks involved with all accelerated tests: Do the failure modes and mechanisms remain the same when the loading conditions are harshened to produce higher acceleration? The purpose of this paper is to answer this question.

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