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Characterization of High-*k* Gate Dielectric with Amorphous Nanostructure

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In the present study, $Zr_xLa_{1-x}O_y$ amorphous nanostructures were prepared by the sol–gel method such that the Zr atomic fraction (x) ranged from 0% to 70%. An analytical model is described for the dielectric constant (k) of $Zr_xLa_{1-x}O_y$ nanostructures in a metal–oxide–semiconductor (MOS) device. The structure and morphology of $Zr_xLa_{1-x}O_y$ film was studied using x-ray diffraction, scanning electron microscopy, atomic force microscopy, and transmission electron microscopy. Elemental qualitative analysis was performed using energy-dispersive x-ray spectra and a map that confirmed the findings. Preliminary information on the influence of thermal annealing on the morphological control of $Zr_xLa_{1-x}O_y$ amorphous nanostructures is presented. The dielectric constant of the crystalline $Zr_{0.5}La_{0.5}O_y$ thin film is about 36. Electrical property characterization was performed using a metal–dielectric–semiconductor structure via capacitance–voltage and current density–voltage measurements.

Key words: CMOS, nanostructures, high-*k* dielectric, sol–gel method

INTRODUCTION

The rapid progress of complementary metal–oxide–semiconductor (CMOS) integrated circuit technology has enabled the Si-based microelectronics industry to simultaneously meet several technological requirements for the expansion of the fuel market. These requirements are performance (speed), low static (off-state) power, and large power supply and output voltages.[1–3] This was accomplished by developing the ability for calculated reduction of the dimensions of fundamental active devices such as field-effect transistors (FETs) in the circuits.[4–6]

It can be argued that the key element enabling scaling of a Si-based metal–oxide–semiconductor FET is the material (and resultant electrical) properties associated with the dielectric employed to isolate the transistor gate from the Si channel in CMOS devices.[7–9] The current CMOS gate dielectric SiO_2 thickness can scale to at least 13 Å, which corresponds to only a four- to five-atom layer, but several problems must be overcome during this process.[10–12] These include dielectric thickness variation, direct tunnel current, penetration of impurities from the gate into the gate dielectric, and the reliability and lifetime of devices made with these films.[13–15]

The physical limitations imposed by SiO_2 have led researchers to study different materials that may comply with the three major requirements of high crystallization temperature, wide energy bandgap, and high dielectric constant.[14] New alternative materials with higher k values than that of SiO_2 (3.9) are needed to form thicker gate dielectrics to achieve the required capacitance. Y_2O_3,[16] Al_2O_3,[17] Ta_2O_5,[18] Gd_2O_3,[19,20] HfO_2,[21] $SrTiO_3$,[22] ZrO_2,[23,24] and La_2O_3[25,26] have received considerable attention as the gate oxide thickness of MOS devices is scaled down.[21,25] Use of an amorphous, high-k material as a gate dielectric offers several key advantages for CMOS processing. These include a (thermodynamically and electrically) stable, high-quality Si–MO_2 interface, a decrease in leakage current according to the Poole–Frenkel emission model,[14] and superior electrical isolation properties.

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