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Four-State Sub-12-nm FETs Employing Lattice-Matched II–VI Barrier Layers

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Three-state behavior has been demonstrated in Si and InGaAs field-effect transistors (FETs) when two layers of cladded quantum dots (QDs), such as SiO_x-cladded Si or GeO_x-cladded Ge, are assembled on the thin tunnel gate insulator. This paper describes FET structures that have the potential to exhibit four states. These structures include: (1) quantum dot gate (QDG) FETs with dissimilar dot layers, (2) quantum dot channel (QDC) with and without QDG layers, (3) spatial wavefunction switched (SWS) FETs with multiple coupled quantum well channels, and (4) hybrid SWS–QDC structures having multiple drains/sources. Four-state FETs enable compact low-power novel multivalued logic and two-bit memory architectures. Furthermore, we show that the performance of these FETs can be enhanced by the incorporation of II–VI nearly lattice-matched layers in place of gate oxides and quantum well/dot barriers or claddings. Lattice-matched high-energy gap layers cause reduction in interface state density and control of threshold voltage variability, while providing a higher dielectric constant than SiO_2. Simulations involving self-consistent solutions of the Poisson and Schrödinger equations, and transfer probability rate from channel (well or dot layer) to gate (QD layer) are used to design sub-12-nm FETs, which will aid the design of multibit logic and memory cells.

Key words: Multistate FETs, four-state QDG FETs, four-state QDSL FETs, four-channel SWS FETs, multiple quantum well/dot channel FETs

INTRODUCTION

High-performance microprocessors use billions of transistors which are approaching sub-12-nm dimensions. A large fraction (50% to 70%) of processor die area is consumed by static random-access memory (SRAM)-based cache.[1] Multichannel spatial wavefunction switched (SWS) field-effect transistors (FETs), quantum dot gate (QDG), and quantum dot channel [or quantum dot superlattice (QDSL) channel] FETs exhibit multistate electrical characteristics and thereby have the potential to process multiple bits simultaneously, resulting in ultracompact (area savings of 50% to 75%) logic circuits and memory devices. This allows high-performance single-chip multicore microprocessors[2,3] to have large on-chip caches that can hold the working sets of the active threads, thereby reducing off-chip memory accesses, or keeping cache sizes constant while reducing area and power consumption.

In terms of sub-12-nm field-effect transistors (FETs), recent studies have ranged from carbon nanotube to graphene devices,[4] nanowire Si and SiGe FETs,[5] and Ge[6] and InGaAs FETs.[7] Double quantum dot structures, laterally coupled by Coulomb blockade barriers involving spin-based quantum computing, have also been reported by a number of investigators,[8,9] including Shaji et al.[10] Spin-based quantum computing using laterally coupled quantum dot-based

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