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Fabrication and Simulation of an Indium Gallium Arsenide Quantum-Dot-Gate Field-Effect Transistor (QDG-FET) with ZnMgS as a Tunnel Gate Insulator

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An indium gallium arsenide quantum-dot-gate field-effect transistor using $Zn_{0.95}Mg_{0.05}S$ as the gate insulator is presented in this paper, showing three output states which can be used in multibit logic applications. The spatial wavefunction switching effect in this transistor has been investigated, and modeling simulations have shown supporting evidence that additional output states can be achieved in one transistor.

Key words: InGaAs MOSFET, high κ, ZnMgS gate dielectric, II–VI insulator, quantum dot gate, multistate behavior

INTRODUCTION

Transistor miniaturization in the semiconductor industry follows Moore's law, which states a 50% size reduction of metal–oxide–semiconductor (MOS) devices every 18 months to 24 months.[1] As transistor size reduces, every design parameter of the transistor will need to shrink to meet the requirement. If the industry is to follow this trend in sub-22-nm silicon technology, the silicon dioxide gate will be less than 20 Å, and this thickness will increase the leakage current in the transistors. Instead of further reducing the silicon dioxide thickness, researchers have started to look into other materials that have a much higher dielectric constant (κ) than silicon dioxide (κ = 3.9). A higher κ means that a thicker gate dielectric can be used to achieve the same performance as with silicon dioxide with the same equivalent oxide thickness (EOT), and use of a thicker gate dielectric can prevent further increase in current leakage of the device.

Research has also been done in developing transistors using materials other than silicon. Indium gallium arsenide (InGaAs) has long been used in high-speed, high-frequency applications of high-electron-mobility transistors (HEMTs) due to its high electron mobility. Chan et al.[2,3] have previously presented InGaAs-based MOS devices utilizing high-κ II–VI materials as the gate insulator stack.

An objective of reducing the size of the transistor is to increase the packing density of the transistors in the final package. More transistors means the storage or bits per unit area will increase. In addition to reducing the size of the transistor, development of field-effect transistors (FETs) that can handle multibit operations can also achieve the same result. One way to accomplish this is to use quantum dots (QDs) at the gate region to manipulate the device threshold voltage. Our research group has presented nonvolatile memory devices using oxide-cladded QDs at the gate as the charge-storage units.[2,4] When electrons tunnel from the inversion channel into the QDs, they remain in the QDs due to the presence of the control gate dielectric, which prevents the charges from leaving through the gate electrode. In a quantum-dot-gate field-

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