

Cu–Cu Hermetic Seal Enhancement Using Self-Assembled Monolayer Passivation

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Low-temperature Cu–Cu thermocompression bonding enabled by self-assembled monolayer (SAM) passivation for hermetic sealing application is investigated in this work. Cavities are etched to a volume of $1.4 \times 10^{-3} \text{ cm}^3$ in accordance with the MIL-STD-883E standard prescribed for microelectronics packaging. The wafer pairs (nonfunctional cavity wafer and cap wafer) are annealed and bonded at 250°C under a bonding force of 5500 N. The encapsulated cavities undergo helium overpressure in a bombing chamber, and the helium leak rate is detected by a mass spectrometer. The measurement results show that the cavities sealed with Cu–Cu bonding after SAM passivation exhibit excellent hermeticity with a leak rate below $10^{-9} \text{ atm cm}^3/\text{s}$, which is an improvement of at least $2\times$ compared with the control sample without SAM passivation.

Key words: Cu–Cu bonding, passivation, self-assembled monolayer, alkanethiol, hermetic, bonding

INTRODUCTION

Three-dimensional (3D) integration has been well recognized and identified for adaptation in future integrated circuit technology scaling to ensure performance enhancement and functional diversification. Three-dimensional integration offers competitive advantages such as enhanced performance, lower cost, form factor reduction, and heterogeneous integration. With 3D integration, dissimilar functional blocks can be stacked to facilitate fabrication processes and improve final system performance. One example is the integration of microelectromechanical system (MEMS) sensors with complementary metal–oxide–semiconductor (CMOS) computation elements for sensing and signal-processing applications. As MEMS structures are in the micron range and are free standing, they require reliable and stable packaging technologies to protect them from

external harsh environments in order to maintain their device performance.¹ Three-dimensional wafer-level packaging offers a relatively simple and low-cost method, as MEMS devices can be packaged in batches and the method can reduce handling damage during assembly. Three-dimensional wafer-level packaging is the process of joining two wafer surfaces together under prescribed loading conditions at specified temperature, pressure, and atmosphere. Bonding techniques such as silicon fusion bonding, anodic bonding, eutectic bonding, thermocompression bonding, adhesive bonding, and glass frit bonding are often employed for wafer-level MEMS packaging.² Compared with these bonding technologies, copper–copper (Cu–Cu) thermocompression bonding presents competitive advantages as the mechanical support, electrical contact, and hermetic seal are formed simultaneously in a single step. Using Cu as a bonding medium is favorable due to a number of reasons: (1) lower cost in comparison with precious metals such as gold, (2) the bonding temperature is in the acceptable range to meet packaging requirements (typically $<300^\circ\text{C}$), and (3) Cu has better

(Received May 29, 2012; accepted November 2, 2012; published online December 6, 2012)