Journal of ELECTRONIC MATERIALS, Vol. 42, No. 7, 2013
DOI: 10.1007/s11664-013-2590-3

High-Temperature Performance of Stacked Silicon Nanowires for Thermoelectric Power Generation

ANDREJ STRANZ,[1] ANDREAS WAAG,[1] and ERWIN PEINER[1,2]

1.—Institute of Semiconductor Technology, TU Braunschweig, University of Technology, Brunswick, Germany. 2.—e-mail: e.peiner@tu-bs.de

Deep reactive-ion etching at cryogenic temperatures (cryo-DRIE) has been used to produce arrays of silicon nanowires (NWs) for thermoelectric (TE) power generation devices. Using cryo-DRIE, we were able to fabricate NWs of large aspect ratios (up to 32) using a photoresist mask. Roughening of the NW sidewalls occurred, which has been recognized as beneficial for low thermal conductivity. Generated NWs, which were 7 μm in length and 220 nm to 270 nm in diameter, were robust enough to be stacked with a bulk silicon chip as a common top contact to the NWs. Mechanical support of the NW array, which can be created by filling the free space between the NWs using silicon oxide or polyimide, was not required. The Seebeck voltage, measured across multiple stacks of up to 16 bulk silicon dies, revealed negligible thermal interface resistance. With stacked silicon NWs, we observed Seebeck voltages that were an order of magnitude higher than those observed for bulk silicon. Degradation of the TE performance of silicon NWs was not observed for temperatures up to 470°C and temperature gradients up to 170 K.

Key words: Silicon thermoelectrics, nanowire array, roughness, thermal conductivity, Seebeck coefficient

INTRODUCTION

Energy harvesting from the large reservoirs of waste heat generated by combustion engines has attracted social and commercial interest, as indicated, for example, by the rapidly increasing market in Japan for thermoelectric power generators (TEGs) from 25 million JPY in 2010 to a forecast 1098 million JPY in 2014.[1] However, the cost per watt and low design temperature of existing materials remain severe obstacles to widespread use of TEGs. Recently, silicon has been recognized as an Earth-abundant, high-production-volume, high-temperature-enduring material for massive recovery of waste heat using TEGs. It was found that the main shortcoming identified so far, namely the low generator thermal resistance caused by the high thermal conductivity of bulk silicon, could be overcome by using rough nanowires (NWs), as supported by theory.[2–5] Meanwhile, fundamental investigations with individual NWs were supported by work with TEGs or TEG-compatible arrays of 10^4 to 10^5 vertical silicon NWs per element.[6–10] Thermal conductivities were reported to be reduced by a factor of 20 compared with bulk, while the Seebeck coefficient and electrical conductivity maintained the favorable values of bulk silicon.[9,10] Top-down approaches based on ultraviolet (UV) lithography and dry etching were used to fabricate NW arrays of uniform height and diameter. However, when using dry etching at room temperature (RT), only short and thin NWs of approximately 1 μm in length and 80 nm to 90 nm in diameter could be generated, thus requiring a thermally and electrically isolating filler material to support the NWs mechanically and enable the top contact in a TEG. Furthermore, testing was performed using integrated heaters at the maximum operating temperature and temperature gradients of 450 K[9,10] and 100 K,[7] respectively, which are far below the ranges available for waste heat recovery, for example, from

(Received July 6, 2012; accepted March 22, 2013; published online April 24, 2013)