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Investigation of Characteristics of Al_2O_3/n-$In_xGa_{1-x}As$ (x = 0.53, 0.7, and 1) Metal–Oxide–Semiconductor Structures

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The electrical properties of Al_2O_3/n-InGaAs metal–oxide–semiconductor capacitors (MOSCAPs) with In content of 0.53, 0.7, and 1 (InAs) have been investigated. Results show small capacitance–voltage (C–V) frequency dispersion in accumulation (1.70% to 1.85% per decade) for these MOSCAPs, mostly being assigned to border traps in Al_2O_3. With higher In content, shorter minority-carrier response time and smaller C–V hysteresis are observed. The reduction of C–V hysteresis might be related to the reduction of Ga-bearing oxides in Al_2O_3/InGaAs interfaces as indicated by x-ray photoelectron spectroscopy.

Key words: ALD Al_2O_3, surface treatment, InGaAs, InAs, MOSCAPs

INTRODUCTION

High-k/III–V structures have been extensively studied recently to realize complementary metal–oxide–semiconductor (MOS) technologies at the 16-nm node and beyond.[1] However, regardless of long-term efforts by the community, the high-k/III–V interface trap density (D_{it}) still remains a challenge. Passivation of high-k/III–V interfaces is always needed to reduce D_{it}. Recently, reports have indicated that the quality of high-k/III–V interfaces not only depends on the passivation method but is also influenced by the III–V compounds themselves.[2,3] Study of high-k/n-InGaAs structures with In content from 0 to 0.53 showed a significant reduction of capacitance–voltage (C–V) frequency dispersion at the accumulation region as the In content reaches 0.53.[3] Besides, some recent reports showed that the frequency dispersion in accumulation in high-k/$In_{0.53}Ga_{0.47}As$ MOS capacitors (MOSCAPs) is closely related to the traps inside the gate oxide, or so-called border traps.[4–6] Simulations have been done on Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSCAPs to study the effect of border traps on the frequency dispersion in the accumulation capacitance.[5,6] In this work, we intend to study the electrical properties of high-k/n-InGaAs structures in which the In content varies from 0.53 to 1. The purpose of the study is to investigate the electrical properties of atomic layer deposition (ALD) Al_2O_3/n-InGaAs MOSCAP structures related to border traps and interface traps, such as the frequency dispersion and hysteresis.

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EXPERIMENTAL PROCEDURES

InGaAs wafers with different In content used in the study were (a) 100 nm $In_{0.53}Ga_{0.47}As$, (b) 5 nm $In_{0.7}Ga_{0.3}As$/10 nm $In_{0.53}Ga_{0.47}$, and (c) 5 nm InAs/3 nm $In_{0.7}Ga_{0.3}As$/10 nm $In_{0.53}Ga_{0.47}As$ epilayer stacks grown on n^+-type InP substrates by molecular beam epitaxy and supplied by IQE Inc. The top layer in each structure was a nominal 2×10^{17} cm^{-3} Si-doped In(Ga)As material. Wafers