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Postgrowth Annealing of CdTe Layers Grown on Si Substrates by Metalorganic Vapor-Phase Epitaxy

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Annealing conditions of CdTe layers grown on Si substrates by metalorganic vapor-phase epitaxy were studied. Typically, 3-μm-thick n-type (211) CdTe layers were annealed for 60 s in flowing hydrogen at atmospheric pressure by covering their surfaces with bulk CdTe wafers. At annealing temperatures above 700°C, improvement of crystal quality was confirmed from full-width at half-maximum values of double-crystal rocking-curve measurements and x-ray diffraction measurements. Photoluminescence measurements revealed no deterioration of electrical properties in the annealed n-CdTe layers. Furthermore, annealing at 900°C improved the performance of radiation detectors with structure of p-like CdTe/n-CdTe/n^+-Si substrate.

Key words: CdTe/Si, MOVPE, rapid thermal annealing, radiation detectors

INTRODUCTION

In this paper we study annealing of CdTe layers grown on Si substrates by metalorganic vapor-phase epitaxy (MOVPE). The large differences in lattice constant and thermal expansion coefficient between CdTe and Si lead to strained layers with high dislocation densities when CdTe layers are grown on Si substrates. The residual strain can cause cracking and peeling-off of the grown layers from the Si substrates. We have developed CdTe heterojunction diode-type radiation detectors that consist of a p-like thick CdTe layer/n-CdTe layer/n^+-Si structure, where the epilayers are grown by MOVPE.[1–6] The thick CdTe layer (p-like) is undoped, high-resistivity material but exhibits p-type conductivity because of growth-induced Cd vacancies. Improvement in the crystal quality of the grown CdTe layers is the main subject of this study, because the performance of such detectors depends on the properties of the grown CdTe layers.

Intensive studies were carried out earlier to grow high-quality CdTe and HgCdTe layers on Si substrates. Different procedures of thermal cyclic annealing of grown layers, and insertions of intermediate ZnTe and/or Ge layers to accommodate the lattice mismatch have been reported.[7–11] These methods, however, are not applicable to our detectors, because insertion of these intermediate layers would create energy barriers at the heterointerface and disturb the carrier transport from the CdTe layers to the Si substrate (vertical direction to the CdTe/Si heterointerface). As an alternative, we employed rapid thermal annealing of n-CdTe layers. The radiation detector was fabricated as follows: A thin n-CdTe buffer layer was first grown on the n^+-Si substrate and then subjected to annealing. Thereafter, the n-CdTe layer was again grown on the annealed layer until its total thickness was typically 5 μm, which was then followed by thick p-like CdTe growth. By annealing, the possibility of peeling-off of the grown CdTe layers was prevented even when their thickness was 300 μm. Also, a decrease in detector dark currents was obtained.[1–6] We studied the effects of annealing on the crystallinity and electrical properties of the grown CdTe layers by changing the annealing temperature.

EXPERIMENTAL PROCEDURES

CdTe layers were grown by using dimethylcadmium and diethyltelluride in a vertical-type MOVPE growth system operating at 1 atm. (211) n^+-Si

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