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PI and PID auto-tuning procedure based on simplified single parameter optimization☆

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ABSTRACT

In this paper a new auto-tuning algorithm for PI and PID controllers based on relay experiments is proposed to minimize the load disturbance integral error (IE) by maximizing the integral gain, subject to a desired phase margin, and a minimum required gain margin constraint. The main advantage of the proposed auto-tuning algorithm with respect to previous works is that it leads, for most of the processes, to PID tuning with close loop performance similar to PID designed using off-line numerical optimization. Moreover the algorithm is applicable to any linear model structure, including dead time and non-minimum phase systems.

1. Introduction

Nowadays most of the commercially available PID controllers include auto-tuning capabilities to simplify the task of determining the controller parameters. In general auto-tuning methods can be classified in two groups: model-based and relay feedback methods. In the former, the tuning is based on simple parametric models of the processes which are obtained from the input/output response. On the other hand, the methods based on relay feedback typically use the information of only one point of the system frequency response, normally where the phase angle is $-\pi$ radians.

The advantages of the relay feedback auto-tuning over model-based algorithms can be summarized as follows: (1) During the experiment the process is under close loop control, therefore the process does not drift away from the nominal operating point. (2) It identifies process frequency response around the ultimate frequency (where the phase angle is $-\pi$ radians) and no previous information about the process model is necessary to get a successful tuning of controllers. Due to this advantages, many authors have been focusing in the improvement of the original Åström and Hägglund method presented in [14]. In this paper a new auto-tuning algorithm for PI and PID controllers based on relay experiments is proposed to minimize the load disturbance integral error (IE) by maximizing the integral gain, subject to a minimum required phase margin, and a minimum required gain margin constraints.

Regarding the design of PID controller minimizing load disturbance, this can be performed either off-line or on-line. The problem of off-line tuning of PID controllers to minimize load disturbance has been widely addressed in the literature. There are some previous works based on the maximization of the integral gain, among these, in [15,8] a direct numerical optimization is proposed, subject to a given value of the maximum of the sensitivity function, while in [16] an approximation of the process to a first-order plus time delay (FOPDT) model is proposed to derive simple tuning rules.

Things are different with auto-tuning of PID controllers. Most of the articles propose design methods to fulfil robustness conditions and/or desired closed-loop bandwidth, see for example [5,6,2]. Only few articles deal with the load disturbance minimization, and the results are quite limited. One of the main causes of this is that the calculation of PID parameters involve a multi-parametric optimization problem with constraints, which can not be easily solved in computers with limited resources, such as the case of embedded controllers where auto-tuning algorithms are implemented. This hurdle was overcome partially in [13] by obtaining formulae for PID and PI parameter calculation to minimize the integral square time error (ISTE) index, using as input data the critical frequency and critical gain measured from a relay feedback experiment. The formulae, however, were obtained for a FOPDT plant model, so the behavior of the process must be approximated by those simple models, and this is not always accurate, leading to a wrong performance.

Recently, in [9], the authors presented a simple procedure to off-line tuning PID controllers through maximizing the integral

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