Robust space vector modulation technique for unbalance voltage disturbances

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ABSTRACT

Space vector modulation (SVM) is one of the most popular PWM techniques used in multilevel inverters. The calculation of reference vector location is very important for SVM technique to obtain exact switching times and to determine correct space vectors. Balanced/unbalanced voltage disturbance occurred in a three-phase system affects the switching times and output voltage of the multilevel inverter. In this study, effects of the disturbances such as line–line faults, balanced and unbalanced voltage sags/swells to SVM technique are investigated and a new technique derived from Clarke transformation is proposed. The effects of disturbances are minimized with this new method. Power System Computer-Aided Design is used to simulate the proposed test system.

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1. Introduction

The increasing number of energy sources and controlled AC drives requires new strategies for the operation and management of the electricity grid in order to maintain or even to improve the power-supply reliability and quality [1]. Controlled AC drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium-voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [2]. These inverters are suitable in high-voltage and high-power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating [3], the increased power ratings and reduced electromagnetic interference (EMI) emission that can be achieved with the multiple DC levels that are available for synthesis of the output voltage waveforms [4].

At the present time, the majority of research and development effort seems to concentrate on the development of three classes of inverters: the diode-clamped multilevel inverter, the multilevel inverter with cascaded single-phase H-bridge inverters and the multilevel inverter known as the flying capacitor inverter or sometimes as the imbricate cells multilevel inverter. The two remaining configurations, namely the multilevel inverter with bi-directional switch interconnections and the multilevel inverter with multiple three-phase inverters are receiving less attention at the present time [5].

Pulse-width modulation (PWM) techniques are gaining importance to control the multilevel inverters for multi-megawatt industrial applications, recently. The output voltage waveforms of the multilevel inverters can be generated at low switching frequencies with high efficiency, low distortion and also harmonics are shifted towards higher frequency bands. In addition, large voltage is easily shared between series devices.

Many different PWM techniques have been developed to achieve aims given in the following [6]:

- wide linear modulation range,
- less switching losses,
- less total harmonic distortion (THD) in the spectrum of switching waveform,
- easy implementation and less computation time.

One of the most popular PWM techniques in the multilevel inverters is space vector modulation (SVM). SVM was originally developed as a vector approach to PWM for three-phase inverters. As SVM has developed, there appears to be some confusion about its characteristics and advantages. Typical claims made for SVM include the following [7]:

- It achieves the wide linear modulation range associated with PWM third-harmonic injection automatically, without the need for distorted modulation.
- It has lower baseband harmonics than regular PWM or other sine-based modulation methods, or otherwise optimizes harmonics.
- Only one switch changes state at a time.

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