ORIGINAL RESEARCH PAPER

A scalable H.264/AVC deblocking filter architecture

T. Cervero · A. Otero · S. López · E. de la Torre · G. M. Callicó · T. Riesgo · R. Sarmiento

Received: 28 December 2012/Accepted: 23 May 2013 © Springer-Verlag Berlin Heidelberg 2013

Abstract The deblocking filter (DF) is one of the most complex functional cores of the H.264/AVC and SVC codecs. Its computational cost is heavily dependent on the video profile and the selected scalability level. With the goal of providing faster and better solutions, developers are focused on designing hardware architectures. Thus, it is possible taking advantage of multitasking, reusability and parallelization techniques. In this context, this work proposes a scalable DF architecture that is able to adapt its structure and performance to different video configurations, due to its modular and regular structure. The scalability feature avoids redesigning the whole architecture in case of the environmental demands or the configuration settings change. These facts mean savings in terms of

T. Cervero (⊠) · S. López · G. M. Callicó · R. Sarmiento Institute of Applied Microelectronics (IUMA), Universidad de Las Palmas de Gran Canaria, 35017 Las Palmas de Gran Canaria, Spain e-mail: tcervero@iuma.ulpgc.es

S. López e-mail: seblopez@iuma.ulpgc.es

G. M. Callicó e-mail: gustavo@iuma.ulpgc.es

R. Sarmiento e-mail: roberto@iuma.ulpgc.es

A. Otero · E. de la Torre · T. Riesgo Center of Industrial Electronics (CEI), Universidad Politécnica de Madrid, 28007 Madrid, Spain e-mail: joseandres.otero@upm.es

E. de la Torre e-mail: eduardo.delatorre@upm.es

T. Riesgo e-mail: teresa.riesgo@upm.es design productivity and silicon area by adapting the necessary logical resources to each condition. Furthermore, regarding the data dependences involved in the H.264/ AVC DF algorithm, the proposed architecture relies on an improved version of a traditional wavefront parallelization strategy, also proposed by the authors. This solution reduces the amount of clock cycles needed to filter a video frame as compared to traditional strategies. Implementation results, in an FPGA Virtex-5, demonstrate the performance benefits of this flexible solution as compared to some rigid state-of-the-art deblocking filter approaches.

Keywords FPGA · Deblocking filter · Scalability · H.264/AVC · Macroblock

1 Introduction

Nowadays, the H.264/AVC video coding standard is one of the most widespread codecs for multimedia applications. This fact is due to its overwhelming features compared to its predecessors, such as a better rate-distortion performance. Unfortunately, the strengths of this codec come at the price of increasing the complexity of the operations and computation. According to [1–4], one of the most time consuming tasks in H.264/AVC and SVC codec standards is the deblocking filter (DF) process, which Table 1 summarizes.

The DF is in charge of reducing blocking artifacts, which appear as a consequence of operations performed in previous functional blocks of the codec chain. As a result, the DF achieves a visual quality improvement of the reconstructed image by smoothing the borders between objects within an image. Furthermore, the processing data arrangement in the DF is hardly subordinated to restrictions imposed by the H.264/AVC [5]. In the case of processing a