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# Buffer structure optimized VLSI architecture for efficient hierarchical integer pixel motion estimation implementation

**Haibing Yin · Dong Sun Park · Xiao Yun Zhang**

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**Abstract** Integer pixel motion estimation (IME) is one crucial module with high complexity in high-definition video encoder. Efficient algorithm and architecture joint design is supposed to tradeoff multiple target parameters including throughput capacity, logic gate, on-chip SRAM size, memory bandwidth, and rate distortion performance. Data organization and on-chip buffer structure are crucial factors for IME architecture design, accounting for multiple target performance tradeoff. In this work, we combine global hierarchical search and local full search to propose hardware efficient IME algorithm, and then propose hardware VLSI architecture with optimized on-chip buffer structure. The major contribution of this work is characterized by: (1) improved hierarchical IME algorithm with presearch and deliberate data organization, (2) multistage on-chip reference pixel buffer structure with high data reuse between integer and fraction pixel motion estimations, (3) highly reused and reconfigurable processing element structure. The optimized data organization and buffer structure achieves nearly 70 % buffer saving with less than average 0.08, 0.12 dB the worst case, PSNR degradation compared with full search based architecture. At the hardware cost of 336 and 382 K logic gate and 20 kB SRAM, the proposed architecture achieves the throughput of 384 and 272 cycles per macroblock, at system frequency of 95 and 264 MHz for 1080p and QFHD @30fps format video coding.

**Keywords** Motion estimation · VLSI architecture · Data organization · Buffer structure

H. Yin (✉)
School of Information Engineering, China Jiliang University, Hangzhou, China
e-mail: yinhb@cjlu.edu.cn

D. S. Park
Division of Electronics and Information Engineering, Chonbuk National University, Jeonju, Jeonbuk, Korea
e-mail: dspark@jbnu.ac.kr

X. Y. Zhang
Institute of Image Communication and Signal Processing, Shanghai Jiaotong University, Shanghai, China
e-mail: xiaoyun.zhang@sjtu.edu.cn

## 1 Introduction

H.264/AVC, VC-1, and AVS video standards achieve superior compression efficiency compared with MPEG-2 and MPEG-4 ASP [1, 2]. Advanced inter-frame prediction techniques, such as variable block size block partition, fraction pixel motion vector, and multiple reference frame inter prediction, contribute to the major compression gain. These coding tools improve the performance at the cost of high complexity. In general, block matching motion estimation consumes 60–70 % computation of the whole encoder, this burden aggravates in high-definition (HD) case due to large search window to cover.

Hardware platforms such as ASIC and FPGA are suitable solutions for HD video encoder implementation. Several works were reported on 720p, 1080p, even quad full high definition (QFHD) H.264/AVC video encoder architectures [3–13]. Integer pixel motion estimation (IME) algorithm and architecture design is the most important task for video codec architecture design.

Full search IME algorithm is well-suited for hardware implementation due to good quality and high regularity [14, 15]. However, it is challenged in HD cases due to large search window and high throughput. Some scholars simplify IME algorithms by reducing search positions,

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